

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Wolfgang Roethig
Assignee: NEC Electronics America, Inc
Title: SYSTEM AND METHOD FOR CALCULATING EFFECTIVE CAPACITANCE FOR TIMING ANALYSIS
Serial No.: Unassigned Filing Date: Herewith
Examiner: Unassigned Group Art Unit: Unassigned
Docket No.: NEC0250US

Austin, Texas

MAIL STOP PATENT APPLICATION
COMMISSIONER FOR PATENTS
P. O. BOX 1450
ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

EXPRESS MAIL NUMBER:

EV 304737505 US

Respectfully submitted,



Brenna A. Brock
Attorney for Applicant(s)
Reg. No. 48,509

U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Serial No.					
		NEC0250US	Unassigned					
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant(s)						
(Use several sheets if necessary)		Wolfgang Roethig						
		Filing Date	Group					
		Herewith	Unassigned					
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
Foreign Patent Documents				Translation				
		Document	Date	Country	Class	Subclass	Yes	No
	AE							
	AF							
	AG							
	AH							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AI	Andrew B. Kahng and Sudhakar Muddu, <i>Proc. IEEE Int'l. Conf. on VLSI Design</i> , "Improved Effective Capacitance Computations For Use In Logic And Layout Optimization," 1999 pp. 578-582.						
	AJ	Kanak Agarwal, Dennis Sylvester and David Blaauw, <i>Design Automation Conference (DAC) '03</i> , "An Effective Capacitance Based Driver Output Model For On-Chip RLC Interconnects," June 2-6, 2003, pp. 376-381.						
	AK	Azeez J. Bhavnagarwala and James D. Meindl, <i>Techcon 2000</i> , "Interconnect Delay Models For Arbitrary Wire-Tree Networks," Microelectronics Research Center and the School of Elec. And Comp. Eng., Georgia Inst. Of Tech., Atlanta, GA.						
	AL							
	AM							
	AN							
	AO							
Examiner		Date Considered						
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								